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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,731	07/31/2001	Mohamed Imam	ONS00187	1255

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EXAMINER	
ROMAN, ANGEL	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 07/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/917,731	Applicant(s) IMAM ET AL.
	Examiner Angel Roman	Art Unit 2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 31 July 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure and Abstract are objected to because of the following informalities: the word "nwell" should be replaced with --n-well-- or --n well--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the device location where the diffused region of the first conductivity type is going to be form.

5. Claim 9 is rejected because of its dependency on rejected claim 8.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 1, 4, 5, 7, 10, 11, 14-16 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Kikuchi et al. U.S. Patent Application Publication 20010036694A1.

Kikuchi et al. discloses a method of manufacturing a semiconductor device comprising; providing a substrate 1 of a first conductivity type; forming a first region 2 of a second conductivity type within the substrate 1 to provide an extended drain region; disposing a first island 8A of field oxide at a top of the substrate within the first region 2; implanting a second region 4 of a first conductivity type in the first region 2, adjacent to

the first island of field oxide 8A; implanting a source diffusion region 11 and a drain diffusion region 12 in the semiconductor device; and annealing the semiconductor device to diffuse the second region, the source diffusion region and the drain diffusion region (see page 3, column 6, lines 10-14).

A second island of field oxide 8B at the top surface of the substrate is formed, within the first region 2, and laterally separated from the first island of field oxide 8A (see figure 5).

Kikuchi et al also discloses forming gate region 10 overlying the first island of field oxide 8A (see figure 6).

Additional regions 7A of the first conductivity type are implanted into the first region (see figure 6).

The drain diffusion region 12 is formed at the surface of the first region 4 (see figure 7).

8. Claims 1, 4, 5, 8-11, 13, 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Sogo U.S. Patent 6,312,996.

Sogo discloses a method of manufacturing a semiconductor device comprising; providing a substrate 31 of a first conductivity type; forming a first region 33 of a second conductivity type within the substrate 31 to provide an extended drain region (see figure 8A); disposing a first island of field oxide 34 at a top of the substrate 31 within the first region 34; implanting a second region 37 of a first conductivity type in the first region 33, adjacent to the first island of field oxide 34; implanting a source diffusion region 40b and

a drain diffusion region 40a in the semiconductor device; and annealing the semiconductor device to diffuse the second region, the source diffusion region and the drain diffusion region (see column 11, lines 45-48).

An insulating layer 38 is applied over the semiconductor device (see figure 8D), the insulating layer 38 having a thickness less than the first island of field oxide 34.

Second islands of field oxide 34 are formed at the top surface of the substrate, within the first region, and laterally separated from the first island of field oxide 34 (see figure 8B).

A gate region 39 is formed overlying the first island of field oxide (see figure 9A).

A diffused region 36 of the first conductivity type is formed adjacent the first region 33 (see figure 9A).

A source diffusion region 40b is formed in the diffused region of the first conductivity type 36 (see figure 9B).

A drain diffusion region 40a is formed at the surface of the first region 33.

9. Claims 1, 2, 3, 11, 12, 15, 18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishibe et al. U.S. Patent 6,399,468 B2.

Nishibe et al. discloses a method of manufacturing a semiconductor device comprising; providing a substrate 101 of a first conductivity type; forming a first region (103, 104) of a second conductivity type within the substrate 101 to provide an extended drain region; disposing a first island 107A of field oxide at a top of the substrate 101 within the first region (103, 104); implanting a second region 105 of a first conductivity

type in the first region (103, 104), adjacent to the first island of field oxide 107A; implanting a source diffusion region 110 and a drain diffusion region 111 in the semiconductor device; and annealing the semiconductor device to diffuse the second region, the source diffusion region and the drain diffusion region.

Nishibe et al. also discloses applying an insulating layer 102 over the semiconductor device, the insulating layer 102 having a thickness less than the first island of field oxide 107A; and implanting the second region 105 of the second conductivity type through the insulating layer (see figure 1).

The step of forming a first region (103, 104) further comprises; forming a first area of first dopant concentration 103 by performing a first area implant; and forming a second area of second dopant concentration 104 different than the first dopant concentration by performing a second area implant, the second area implant is laterally offset from the first area (see figure 2).

Second field oxide regions 107B are also formed (see figure 5).

10. Claims 1, 4, 6 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi U.S. Patent 6,346,448.

Kobayashi discloses a method of manufacturing a semiconductor device comprising; providing a substrate of a first conductivity type PSUB; forming a first region of a second conductivity type NWELL within the substrate PSUB to provide an extended drain region; disposing a first island of field oxide 420 at a top of the substrate within the first region; implanting a second region PWELL of a first conductivity type in the first

region NWELL, adjacent to the first island of field oxide 420; implanting a source diffusion region and a drain diffusion region 412 in the semiconductor device; and annealing the semiconductor device to diffuse the second region, the source diffusion region and the drain diffusion region.

Second islands of field oxide 420 are formed at the top surface of the substrate, within the first region, and laterally separated from the first island of field oxide (see figure 7A).

Conductive regions 431 are formed overlying the second islands of field oxide.

As to the language used in claims 1, 11, and 15 "to balance charges in the first region", applicant should note that this is merely "result" language which cannot be relied upon to define over the references (Kikuchi et al., Sogo, Nishibe et al. and Kobayashi), since the references disclosed all of the claimed steps and their recited relationships. Moreover, the examiner will presume that the recited results are inherent in the references, since all of the claimed steps and the relationship therebetween are meet by the references.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Evans, Seki, Moyer et al. and Chien et al. disclosed methods of making MOS transistor devices by implanting regions of different conductivity types in semiconductor devices.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
July 14, 2002

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800